

**WHAT IS CLAIMED IS:**

1           1.       A method for optimizing buffers in an integrated circuit design  
2 comprising:  
3           identifying paths and nodes within the integrated circuit design;  
4           determining node overlap within the integrated circuit design;  
5           calculating possible solutions for addressing timing violations within the  
6                       integrated circuit design;  
7           choosing a solution for addressing timing violations;  
8           inserting buffers at particular nodes of the integrated circuit design; and,  
9           repeating the calculating possible solutions, the choosing a solution and the  
10                       inserting buffers at particular nodes to address timing violations within  
11                       the integrated circuit design.

1           2.       The method for optimizing buffers in an integrated circuit design of  
2 claim 1 wherein  
3           the repeating continues until a previous maximum number of violations have  
4                       been addressed.

1           3.       The method for optimizing buffers in an integrated circuit design of  
2 claim 2 wherein  
3           after the repeating, there are orphan timing violations remaining to be  
4                       addressed; and, further comprising  
5           inserting buffers at particular locations to address the orphan timing violations.

1           4.       The method for optimizing buffers in an integrated circuit design of  
2 claim 1 wherein  
3           the choosing a solution is based upon fixing a plurality of timing violations  
4                       based upon various input criteria.

1           5.     The method for optimizing buffers in an integrated circuit design of  
2 claim 4 wherein  
3           the various input criteria include a median approach, the median approach  
4           including calculating a nominal number of fixes from the calculating  
5           possible solutions and then selecting an approach which fixes more  
6           than the nominal number of fixes.

1           6.     The method for optimizing buffers in an integrated circuit design of  
2 claim 4 wherein  
3           the various input criteria include an acquisitive approach, the acquisitive  
4           approach including determining which solution from the calculating  
5           possible solutions fixes a greatest number of timing violations and then  
6           selecting the approach which fixes the greatest number of timing  
7           violations.

1           7.     The method for optimizing buffers in an integrated circuit design of  
2 claim 1 further comprising:  
3           identifying buffers from a list of potential buffers available to insert into the  
4           integrated circuit design; and  
5           choosing a subset of the buffers from the list as buffers for inserting at the  
6           particular nodes of the integrated circuit.

1           8.     The method for optimizing buffers in an integrated circuit design of  
2 claim 7 wherein:  
3           factors used in choosing a subset of the buffers from the list as buffers include  
4           a first order delay characteristic of the buffer, a maximum time slack  
5           characteristic of the buffer, and a drive strength characteristic of the  
6           buffer.

1           9.     A apparatus for optimizing buffers in an integrated circuit design  
2 comprising:  
3           means for identifying paths and nodes within the integrated circuit design;

4 means for determining node overlap within the integrated circuit design;  
 5 means for calculating possible solutions for addressing timing violations  
 6 within the integrated circuit design;  
 7 means for choosing a solution for addressing timing violations;  
 8 means for inserting buffers at particular nodes of the integrated circuit design;  
 9 and,  
 10 means for repeating the calculating possible solutions, the choosing a solution  
 11 and the inserting buffers at particular nodes to address timing  
 12 violations within the integrated circuit design.

1 10. The apparatus for optimizing buffers in an integrated circuit design of  
 2 claim 9 wherein  
 3 the repeating continues until a previous maximum number of violations have  
 4 been addressed.

1 11. The apparatus for optimizing buffers in an integrated circuit design of  
 2 claim 10 wherein  
 3 after the repeating, there are orphan timing violations remaining to be  
 4 addressed; and, further comprising  
 5 means for inserting buffers at particular locations to address the orphan timing  
 6 violations.

1 12. The apparatus for optimizing buffers in an integrated circuit design of  
 2 claim 9 wherein  
 3 the choosing a solution is based upon fixing a plurality of timing violations  
 4 based upon various input criteria.

1 13. The apparatus for optimizing buffers in an integrated circuit design of  
 2 claim 12 wherein  
 3 the various input criteria include a median approach, the median approach  
 4 including calculating a nominal number of fixes from the calculating  
 5 possible solutions and then selecting an approach which fixes more  
 6 than the nominal number of fixes.

1           14.    The apparatus for optimizing buffers in an integrated circuit design of  
2 claim 12 wherein  
3           the various input criteria include an acquisitive approach, the acquisitive  
4           approach including determining which solution from the calculating  
5           possible solutions fixes a greatest number of timing violations and then  
6           selecting the approach which fixes the greatest number of timing  
7           violations.

1           15.    The apparatus for optimizing buffers in an integrated circuit design of  
2 claim 9 further comprising:  
3           means for identifying buffers from a list of potential buffers available to insert  
4           into the integrated circuit design; and  
5           means for choosing a subset of the buffers from the list as buffers for inserting  
6           at the particular nodes of the integrated circuit.

1           16.    The apparatus for optimizing buffers in an integrated circuit design of  
2 claim 15 wherein:  
3           factors used in choosing a subset of the buffers from the list as buffers include  
4           a first order delay characteristic of the buffer, a maximum time slack  
5           characteristic of the buffer, and a drive strength characteristic of the  
6           buffer.

1           17.    A system for optimizing buffers in an integrated circuit design  
2 comprising:  
3           an identifying module, the identifying module identifying paths and nodes  
4           within the integrated circuit design;  
5           a determining module, the determining module determining node overlap  
6           within the integrated circuit design;  
7           a calculating module, the calculating module calculating possible solutions for  
8           addressing timing violations within the integrated circuit design;  
9           a choosing module, the choosing module choosing a solution for addressing  
10          timing violations;

11 an inserting module, the inserting module inserting buffers at particular nodes  
 12 of the integrated circuit design; and,  
 13 a repeating module, the repeating module repeating the calculating possible  
 14 solutions, the choosing a solution and the inserting buffers at particular  
 15 nodes to address timing violations within the integrated circuit design.

1 18. The system for optimizing buffers in an integrated circuit design of  
 2 claim 17 wherein  
 3 the repeating continues until a previous maximum number of violations have  
 4 been addressed.

1 19. The system for optimizing buffers in an integrated circuit design of  
 2 claim 18 wherein  
 3 after the repeating, there are orphan timing violations remaining to be  
 4 addressed; and, further comprising  
 5 an orphan inserting module, the orphan inserting module inserting buffers at  
 6 particular locations to address the orphan timing violations.

1 20. The system for optimizing buffers in an integrated circuit design of  
 2 claim 18 wherein  
 3 the choosing a solution is based upon fixing a plurality of timing violations  
 4 based upon various input criteria.

1 21. The system for optimizing buffers in an integrated circuit design of  
 2 claim 20 wherein  
 3 the various input criteria include a median approach, the median approach  
 4 including calculating a nominal number of fixes from the calculating  
 5 possible solutions and then selecting an approach which fixes more  
 6 than the nominal number of fixes.

1           22.    The system for optimizing buffers in an integrated circuit design of  
2 claim 20 wherein  
3           the various input criteria include an acquisitive approach, the acquisitive  
4           approach including determining which solution from the calculating  
5           possible solutions fixes a greatest number of timing violations and then  
6           selecting the approach which fixes the greatest number of timing  
7           violations.

1           23.    The system for optimizing buffers in an integrated circuit design of  
2 claim 9 further comprising:  
3           an identifying module, the identifying module identifying buffers from a list of  
4           potential buffers available to insert into the integrated circuit design;  
5           and  
6           a subset choosing module, the subset choosing module choosing a subset of  
7           the buffers from the list as buffers for inserting at the particular nodes  
8           of the integrated circuit.

1           24.    The system for optimizing buffers in an integrated circuit design of  
2 claim 23 wherein:  
3           factors used in choosing a subset of the buffers from the list as buffers include  
4           a first order delay characteristic of the buffer, a maximum time slack  
5           characteristic of the buffer, and a drive strength characteristic of the  
6           buffer.